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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,842	10/14/2003	Ken Gary Pomaranski	200310434-1	3525

22879 7590 11/28/2007

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EXAMINER	
WU, JUNCHUN	
ART UNIT	**PAPER NUMBER**
2191	
MAIL DATE	**DELIVERY MODE**
11/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,842	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Junchun Wu	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 14, 2007 has been entered.

2. Applicant's amendment dated September 14, 2007, responding to the Office action dated June 11, 2007 provided in the rejection of claims 1-25, wherein claim 3 has been amended.

Claims 1-25 remain pending in the application and which have been fully considered by the examiner.

Applicant's arguments with respect to claims rejection have been fully considered but are moot in view of the new grounds of rejection - see Killian et al., art made of record, as applied hereto.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-8, 15,17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (US Patent No. 6,760,888 B2, hereinafter "Killian"), Colwell et al. (US Patent No. 4,833,599, hereafter "Colwell").

3. Per claim 1 (previously presented)

Killian discloses

A method of compiling a program to be executed on a target microprocessor with multiple execution units of a same type (Abstract "... *development tools such as a compiler, assembler, debugger and simulator which can be used to develop applications for the processor and to verify it.*"), the method comprising:

But Killian does not disclose

- selecting, by a program compiler, one of the execution units for testing and scheduling, by the program compiler, execution of diagnostic code on the selected execution unit; and scheduling, by the program compiler, execution of program code on remaining execution units of the same type and execution of diagnostic code on the selected execution unit and said execution of program code on the remaining execution units are scheduled to be performed in parallel

However Colwell discloses

- selecting, by a program compiler, one of the execution units for testing (col.7 lines 5-12 *"The compiler uses various methods to select the best of the multiple projected traces and calls..."*).

- scheduling, by the program compiler, execution of diagnostic code on the selected execution unit; and scheduling, by the program compiler, execution of program code on remaining execution units of the same type (col.2 lines 45-58 *"selected plurality of instructions including at most on branch instruction... "* & col.3 lines 15-20 *"Each processing cluster features, for executing a branch instruction, circuitry responsive to the instruction data directed for testing... "*).
- wherein said execution of diagnostic code on the selected execution unit and said execution of program code on the remaining execution units are scheduled to be performed in parallel (col.3 lines 5-15).
- Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify teaching of Killian with the teachings of Colwell to include those descriptions above in order to provide a method for simultaneously executing a plurality of sequential instructions in a parallel processor (col.1 lines 58-68).

4. Per claim 3 (currently amended)

the rejection of claim 1 is incorporated and Killian further discloses

- source code is input into the program compiler, object code is output from the program compiler, and wherein said scheduling is performed by the program compiler prior to execution of the object code by the target microprocessor (col.8 lines 25-27 *"inputs to the instruction scheduling logic of the processor to make sure the instruction issues only when its operands are valid"* i.e. all the inputs are add to the application-specific instructions before the object code is executed.

5. For claim 4 (original)

the rejection of claim 1 is incorporated and Colwell further discloses

- setting a level of aggressiveness for scheduling the testing of the execution units (col.11 lines 25-26; each cluster is assigned a priority level).

6. For claim 5 (original)

the rejection of claim 4 is incorporated and Colwell further discloses

- applying an aggressiveness-dependent algorithm to determine when to schedule all available units for execution of the program code and when to schedule parallel execution of the program code and the diagnostic code (col.22 lines 24-32).

7. For claim 6 (original)

the rejection of claim 5 is incorporated and Colwell further discloses

- a lowest level of aggressiveness comprises turning off said testing (col.11 lines 31-34; This two bit field represents the state of bus usage by the processor. e.g. if last two bits equal to 11, the bus is unavailable for that processor).

8. For claims 7 (original) and 17 (previously presented)

the rejection of claim 1 is incorporated and Colwell further discloses

- the multiple execution units of the same type comprise arithmetic logic units (col.5 lines 49-53 & see Fig.3 70,72).

9. For claims 8 (original) and 18 (previously presented)

the rejection of claim 1 is incorporated and Colwell further discloses

- the multiple execution units of the same type comprise floating point units (col.6 lines 10-12).

10. Per claim 15 (previously presented)

Colwell further discloses

A computer-readable medium having a program product for execution on a target microprocessor having multiple execution units of a same type integrated thereon (col.6 lines 46-49), the program product comprising:

microprocessor-executable diagnostic code stored on the computer-readable medium and configured by a program compiler to be executed on a selected execution unit of the multiple execution units (col.2 lines 36-44).

- microprocessor-executable program code stored on the computer-readable medium and configured by the program compiler to be executed on remaining execution units of the same type (col.2 lines 45-58 *"selected plurality of instructions including at most on branch instruction... "* & col.3 lines 15-20 *"Each processing cluster features, for executing a branch instruction, circuitry responsive to the instruction data directed for testing... "*).
- wherein said diagnostic code and said program code are scheduled to be performed in parallel on the selected execution unit and the remaining execution units, respectively

(col.3 lines 5-15 *"each instruction of a group being executed in a parallel processing fashion..."*).

11. Claims 9-14, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian, in view of Colwell and further view of Raina (US Patent No. 6,134,675).

12. For claims 9 (original) and 19 (previously presented)

the rejection of claims 1 and 15 are incorporated

Both Killian and Colwell do not disclose

- the multiple execution units comprise at least four execution units of the same type integrated onto the microprocessor integrated circuit.

But Raina discloses

- the multiple execution units comprise at least four execution units of the same type integrated onto the microprocessor integrated circuit (Fig 1 & col.2 lines 7-10).
- Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Killian and Colwell and further include the multiple execution units comprise at least four execution units of the same type integrated onto the microprocessor integrated circuit by teaching of Raina in order to improve the method for testing multi-core processor integrated circuits (Raina col.1 lines 22-23).

13. For claims 10 (original) and 20 (previously presented)

the rejection of claims 1 and 15 are incorporated

Both Killian and Colwell do not disclose

- the scheduled diagnostic code performs diagnostic operations from a test pattern comprising operations with known expected results.

But Raina discloses

- the scheduled diagnostic code performs diagnostic operations from a test pattern comprising operations with known expected results (col.3 lines 19-22).
- Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Killian and Colwell and further include the scheduled diagnostic code by performing diagnostic operations from a test pattern comprising operations with known expected results by teaching of Raina in order to improve method that is better suited for testing integrated circuits containing multiple cores (Raina col.1 lines 22-23).

14. For claims 11 (original) and 21 (previously presented)

the rejection of claims 10 and 20 are incorporated and Raina further discloses

- the scheduled diagnostic code compares an actual result with a known expected result (Raina col.3 lines 19-22).

15. For claims 12 (original) and 22 (previously presented)

the rejection of claims 11 and 21 are incorporated and Raina further discloses

- the scheduled diagnostic code jumps to a fault handler if the compared results are different (col.3 lines 15-22).

16. For claims 13 (original) and 23 (previously presented)

the rejection of claims 12 and 22 are incorporated and Raina further discloses

- the fault handler includes code to remove a faulty execution unit from use in executing code (col.3 lines 17-19).

17. For claims 14 (original) and 24 (previously presented)

the rejection of claims 12 and 22 are incorporated and Raina further discloses

- the fault handler includes code to perform a system halt to prevent data corruption (col.3 lines 17-19).

18. Claims 2, 16, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian, in view of Colwell and further view of Murthi et al. (US Patent No. 5,673,388, hereafter Murthi).

19. Per claim 2 (original)

the rejection of claim 1 is incorporated

Both Killian and Colwell do not disclose

- the selection of the execution unit for testing utilizes an algorithm that assures testing of each of the multiple execution units,

But Murthi discloses

- the selection of the execution unit for testing utilizes an algorithm that assures testing of each of the multiple execution units (col.7 lines 44-53 & Fig. 2; col.9 lines 56-57).

- Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Killian and Colwell and further include utilizing an algorithm that assures testing of each of the multiple execution units as taught by Murthi in order to provide a faster way of initializing a multiple processor computer system and increase the speed of testing in the multiple processor system (Murthi col.2 lines 11-13).

20. Per claim 16 (previously presented)

the rejection of claim 15 is incorporated

Both Killian and Colwell do not disclose

- the selected execution unit rotates between the multiple execution units such that each execution unit is tested.

But Murthi discloses

- the selected execution unit rotates between the multiple execution units such that each execution unit is tested (col.7 lines 44-53 & Fig. 2; in a multiprocessor system, bootstrap processor (BSP) oversee the initialization and perform the bulk of initialization tests for each processor other than BSP).
- Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Killian and Colwell and further include the selected execution unit rotates between the multiple execution units such that each execution unit is tested as taught by Murthi in order to provide a faster way of initializing

a multiple processor computer system and increase the speed of testing in the multiple processor system (Murthi col.2 lines 11-13).

21. Per claim 25 (previously presented)

Colwell discloses

A computer-readable medium having a program product for execution on a target microprocessor having multiple execution units of a same type integrated thereon (col.6 lines 46-49), the program product comprising:

- microprocessor-executable diagnostic code stored on the computer-readable medium and scheduled by a program compiler to be executed on a selected execution unit of the multiple execution units (col.7 lines 5-12 *"The compiler uses various methods to select the best of the multiple projected traces and calls..."*).
- microprocessor-executable program code stored on the computer-readable medium and scheduled by the program compiler to be executed on remaining execution units at a same time as the diagnostic code is to be executed on the selected execution unit (col.2 lines 45-58 *"selected plurality of instructions including at most on branch instruction..."* & col.3 lines 15-20 *"Each processing cluster features, for executing a branch instruction, circuitry responsive to the instruction data directed for testing..."*).
- wherein said diagnostic code is further configured to be run in a background type process on a multi-threaded operating system (col.6 lines 61-65)

But Colwell does not disclose

- the selected execution unit rotates between the multiple execution units such that each execution unit is tested.

However, Murthi teaches

- the selected execution unit rotates between the multiple execution units such that each execution unit is tested (col.7 lines 44-53 & Fig. 2; in a multiprocessor system, bootstrap processor (BSP) oversee the initialization and perform the bulk of initialization tests for each processor other than BSP).
- Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Colwell's teachings by the selected execution unit rotates between the multiple execution units such that each execution unit is tested as taught by Murthi in order to provide a faster way of initializing a multiple processor computer system and increase the speed of testing in the multiple processor system (Murthi col.2 lines 11-13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junchun Wu whose telephone number is 571-270-1250. The examiner can normally be reached on 8:00-17:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JW

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SUPERVISORY PATENT EXAMINER